AMENDMENT

In the Claims:

Please amend claims 1 and 16; and add new claims 33-36, as follows:

1. (Currently Amended) An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer that comprises metal regions disposed between dielectric regions;

a protective overcoat formed over the metallization layers, the protective overcoat having vias through it;

tungsten plugs substantially filling the vias and connecting to one of the metal regions in the uppermost layer; and

thick copper formed over the protective overcoat and forming connections to the tungsten plugs.

2. (Original) The integrated circuit of claim 1, wherein the uppermost layer is an aluminum metallization layer.

3. (Original) The integrated circuit of claim 1, wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers.

4. (Cancelled).

5. (Cancelled).

6. (Cancelled).

7. (Original) The integrated circuit of claim 1, wherein the thick copper forms interconnections between device elements within the integrated circuit.

8. (Cancelled)

9. (Cancelled).

10. (Cancelled).

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Currently Amended) An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements, the one or more metallization layers having an uppermost layer, the uppermost layer comprising bond pads;

a protective overcoat formed over the metal layers, the protective overcoat having vias through it, wherein ~~arrays of~~ multiple vias are formed over individual bond pads;

metal plugs substantially filling the vias and connecting to the bond pads; and

thick copper connections to the metal plugs.

17. (Original) The integrated circuit of claim 16, wherein the metal plugs are copper plugs.

18. (Cancelled).

19. (Original) The integrated circuit of claim 16, wherein the metal plugs have a coefficient of thermal expansion less than or equal to about 8 ppm/°C.

20. (Original) The integrated circuit of claim 16, wherein the metal plugs are tungsten plugs.

21. (Original) The integrated circuit of claim 16, wherein the uppermost layer is an aluminum metallization layer.

22. (Original) The integrated circuit of claim 16, wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers.

23. (Original) The integrated circuit of claim 16, wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

24. (Cancelled)

25. (Cancelled)

26. (Cancelled).

27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Cancelled).

33. (New) The method of claim 1, wherein some of the metal plugs couple at least one of the thick copper connections to one of the metal regions.

34. (New) The method of claim 1, wherein the thick copper substantially overlies at least one of the metal regions.

35. (New) The method of claim 1, wherein the thick copper does not extend over at least a portion of at least one of the dielectric regions.

36. (New) The method of claim 16, wherein the multiple metal plugs individually couple the thick copper connections to the bond pads.